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METHOD AND APPARATUS FOR INCREASING THE DEVICE COUNT ON A SINGLE ATA BUS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims pPriority ~~is claimed~~ from U.S. Provisional Patent Application Serial No. 60/210,713, filed June 9, 2000 entitled "Increasing the Disk Drive Count on a Single ATA Bus~~INCREASING THE DISK DRIVE COUNT ON A SINGLE ATA BUS,~~" which is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates to increasing the device count on a single ATA bus. In particular, the present invention allows more than two devices to be ~~inter~~connected to a single ~~channel of an~~ ATA bus.

BACKGROUND OF THE INVENTION

Various host computers (and m~~M~~ost personal computers) include~~are provided with~~ an Advanced Technology Attachment (ATA) controller for communicating with ATA ~~allowing various~~ devices ~~to communicate with the host system~~ using an ATA bus. T~~In a typical system, t~~he ~~ATA~~ controller typically has ~~is provided with~~ two channels, each of which is connected to an ATA bus, and each ATA bus can be connected to ~~are~~

~~capable of interconnecting to~~ two devices. The host computer can include additional controllers to connect to more devices~~In order to increase the number of devices that can be connected to the host system, it is possible to add additional ATA controllers~~. However, ~~the~~ additional ~~number of~~ controllers ~~that can be added to any one system is limited, provision of the additional controllers~~ adds ~~to the~~ cost, do not allow for command overlapping between devices and do not improve performance. Furthermore, ~~of the system, and providing~~ appropriate cabling is difficult. ~~In addition, such an approach it does not allow for command overlapping between devices and having additional controllers does not improve performance.~~

Alternative bus protocols~~As an alternative to an ATA bus for connecting devices to a host system, other bus protocols~~ are available. For instance, the small computer system interface (SCSI) allows ~~as many as~~ 255 SCSI devices to be ~~inter~~connected to a single SCSI bus. However, SCSI devices are expensive, and the~~an~~ SCSI controller~~, which~~ is not normally provided in a personal ~~as part of a PC type~~ computer~~, must be used~~. Furthermore, although ~~the~~ SCSI ~~type bus provides~~ improve~~s~~d performance over ATA, the SCSI data rate ~~of such a bus~~ cannot be fully exploited by most host computer~~systems~~s and SCSI devices.

Accordingly, it would be advantageous to ~~provide a low cost method and apparatus to~~ increase the number of devices that can be ~~inter~~connected to a single ~~channel of an~~ ATA bus.

~~In addition, it would be advantageous to provide such a method and apparatus that was reliable in operation and that offered performance advantages over a standard ATA type interconnection.~~

SUMMARY OF THE INVENTION

~~In accordance with the present invention, a method and an apparatus for increasing the drive count on a single ATA type bus are provided.~~ The present invention allows more than two devices to be ~~inter~~connected to a single ATA ~~type~~ bus.

In accordance with an embodiment of~~.~~ ~~According to~~ the present invention, the ~~each~~ devices are each~~is~~ assigned a unique identifier, and ~~and~~ the controller selects a device by sending ~~is selected by~~ a selection command that includes a selection identifier across~~provided using the~~ data lines of the ATA ~~type~~ bus to the devices. The devices each receive the selection command and compare the selection identifier to the assigned identifier. The device which matches the selection identifier to its assigned identifier is selected, and the other devices are not selected. The selected device prepares to receive an additional command or data from the ATA bus, and the other devices disconnect themselves from the ATA bus.

In accordance with another~~one~~ embodiment of the present invention, the selected device updates its status register and asserts PDIAG and INTRQ in response to the selection command, and the controller reads the status register of the selected device to verify proper device selection in response to the PDIAG and INTRQ assertions~~a modified ATA~~.

In accordance with another embodiment of the present invention, the controller includes DASP, PDIAG and INTRQ registers, the ATA bus includes multiple DASP, PDIAG and INTRQ lines connected to the DASP, PDIAG and INTRQ registers, and the devices share the data lines but have dedicated DASP, PDIAG and INTRQ lines.

In accordance with another embodiment of the present invention, the controller includes DASP, PDIAG and INTRQ registers, the ATA bus includes multiple DASP, PDIAG and INTRQ lines connected to the DASP, PDIAG and INTRQ registers, and the devices share the data lines and the DASP, PDIAG and INTRQ lines.

Advantageously, ~~type cable having a terminal for interconnecting the cable to a modified ATA controller, and having at least three terminals for interconnecting the modified ATA type cable to at least three modified ATA devices is provided. The controller selects one of the devices by issuing a selection command. Each device interconnected to the ATA type bus receives the selection command, and compares an identifier provided with the selection command to an assigned identifier for that device. The selected device prepares itself to receive an additional command or data, while those devices that are not selected disconnect themselves from the modified ATA type bus.~~

~~According to another embodiment of the present invention, each device to be interconnected to a modified ATA type controller is provided with a different identifier. In operation, the controller issues a selection command that includes an identifier corresponding to one of the assigned identifiers. In response to receiving the selection command, the selected device prepares to receive an additional command or data, while those devices that were not selected disconnect themselves from the modified ATA bus.~~

~~According to an embodiment of the present invention, as many as 256 devices may be interconnected to a single modified ATA type channel. According to another embodiment of the present invention, as many as eight devices may be interconnected to a single channel of a modified ATA type bus.~~

~~In accordance with still another embodiment of the present invention, a device~~

~~suitable for use in connection with the present invention includes a standard ATA type device that has been modified to compare a received identifier to an assigned identifier in response to receiving a selection command. A controller suitable for use in connection with the present invention may be an ATA type controller modified to issue a selection command using data lines provided as part of the ATA bus. A cable or interconnection suitable for use in connection with the present invention may be an ATA cable modified to allow more than two devices to be interconnected to the modified ATA type controller.~~

~~Based on the foregoing summary, a number of salient features of the present invention are readily discerned. A method and an apparatus for increasing the device count of a single ATA type bus are provided. In particular, the method and apparatus of the present invention allow more than two devices to be interconnected to a single modified ATA bus. In addition, the method and apparatus of~~ the present invention allows ~~the interconnection of~~ more than two devices to be connected to a single ATA bus~~channel~~ with only slight modifications to the ~~operating parameters of an ATA controller~~bus system~~and ATA type device, and with the provision of an ATA type cable, modified to provide terminals for the desired number of devices~~.

Additional advantages of the present invention will become readily apparent from the following discussion, particularly when taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating a computer system that includes a bus system with a controller, an ~~utilizing a modified~~ ATA bus and devices ~~in accordance with the~~

~~present invention~~;

Fig. 2 is a flowchart illustrating ~~the~~ operational steps taken during power-up of the bus system without additional hardware~~an embodiment of the present invention~~;

Fig. 3 is a flowchart illustrating operational steps taken by a device in response to a ~~device~~ selection command that includes determining whether the bus system includes additional hardware ~~in accordance with an embodiment of the present invention~~;

Fig. 4 is a flowchart illustrating operational steps taken during device selection without additional hardware in the bus system ~~in accordance with an embodiment of the present invention~~;

Fig. 5 is a block diagram illustrating the additional hardware in the bus system~~suitable for use in connection with an embodiment of the present invention~~;

Fig. 6 is a flowchart illustrating operational steps taken during power-up of the bus system with the additional hardware~~yet another embodiment of the present invention~~; and

Fig. 7 is a flowchart illustrating operational steps taken during device ~~drive~~ selection with the additional hardware in the bus system ~~in accordance with yet another embodiment of the present invention~~.

DETAILED DESCRIPTION

Fig. 1 illustrates in block diagram form a computer system **100** that includes a host computer **104** and ~~utilizing~~ a ~~modified ATA~~ bus system ~~**104** having an increased device count in accordance with an embodiment of the present invention. In addition to the modified ATA bus system **104**, the system **100** includes a host computer~~ **106**. The

host computer **104**~~6~~ ~~generally~~ includes a system bus **108**, a processor **112**, ~~and~~ system memory **116** and a controller **120**.

The ~~modified ATA~~ bus system **106**~~4~~ ~~generally~~ includes the ~~a modified ATA interface or~~ controller **120**, a single ~~modified~~ ATA bus **124** and ~~a plurality of modified ATA~~ devices **128** designated as devices **128-0**~~a~~, **128-1**~~b~~, **128-2**~~c~~, **128-3**~~d~~, **128-4**~~e~~, **128-5**~~f~~, **128-6**~~g~~, and **128-7**~~h~~. Thus, the host computer **104** and the bus system **106** share the controller **120**~~In general, the components of the modified ATA bus system 104 in accordance with the present invention are altered as compared to the components used in connection with a conventional ATA bus as described in detail below~~.

The ~~modified ATA interface or~~ controller **120** provides an ATA interface that ~~generally serves to inter~~connects the system bus **108** to ~~to~~ the ~~various devices 128 via the modified~~ ATA bus **124**. Thus, ~~In general,~~ the ~~modified ATA~~ controller **120** translates between the protocols of the system bus **108** and the ~~protocol of the~~ ATA bus ~~(or input/output bus)~~ **124**. T~~In a typical ATA controller, no more than two devices may be interconnect to each of the provided first and second channels. However, t~~he controller **120** also ~~of the present invention is cap~~connects the system bus **108** to the devices **128** via the ATA bus **124**~~able of having more than two devices 128 interconnected to a single channel~~.

The ATA bus **124** includes the ATA signal lines such as data lines and the DASP (device active, slave present), PDIAG (passed diagnostic) and INTRQ (interrupt request) lines under the ATA protocol. Likewise, the signal lines are terminated under the ATA protocol. The ATA bus **124** also includes a ribbon cable, a ribbon connector connected to the controller **120** and edge connectors connected to the devices **128**. However, unlike a

conventional ATA bus, the ATA bus **124** has eight edge connectors (rather than two) to provide separate edge connectors for each of the eight devices **128**.

The devices **128** are ATA storage devices such as hard disk drives, floppy drives, optical drives and tape drives. The devices **128** include ATA connection pins such as data, DASP, PDIAG and INTRQ connection pins for connecting with the corresponding signal lines in the ATA bus **124**. Furthermore, the devices **128** are each assigned a unique identifier. The identifiers may be assigned through hardware or software. For example, the identifiers may be assigned using jumpers on the exteriors of the devices **128**. Alternatively, the identifiers may be assigned by setting software switches during the initialization of the devices **128**.

The host computer **104** can perform ATA command and data transfer operations across the ATA bus **124** with any of the devices **128**. The controller **120** sends a selection command that includes a selection identifier over the data lines to the devices **128**. The selection command can be issued at any time the data lines are available, and need not be issued during a selection phase, a command phase or a resolution phase. The devices **128** share the data lines and therefore receive the selection command and its selection identifier from the ATA bus **124**. The ~~Briefly stated, the firmware of the controller **120** of the present invention is modified from a controller in accordance with a conventional ATA bus in that the controller **120** of the present invention is capable of sending a selection command over data lines provided as part of the ATA bus **124** prior to issuance of a command or data directed to the selected device **128**.~~

~~The modified ATA bus **124** of the present invention is, according to one embodiment of the present invention, identical to a conventional ATA bus, in that the~~

~~modified ATA bus 124 includes an 8-bit data bus, and signal lines for each of the DASP, PDIAG and IRQ signals. In addition, the conductors used to provide above-mentioned data bus and signal lines are terminated in connectors provided in accordance with the ATA protocol. However, unlike a conventional ATA bus, the modified ATA bus 124 of the present invention may be provided with more than two terminals to which devices 128 may be interconnected. According to one embodiment of the present invention, the modified ATA bus 124 is provided with terminals for interconnecting as many as eight devices 128 to the bus 124 and in turn to the controller 120. According to another embodiment of the present invention, a modified ATA bus 124 having decoding logic may receive individual DASP, PDIAG and IRQ signals and may feed those signals to registers in the controller 120, as will be explained in greater detail below.~~

~~According to still another embodiment of the present invention, as many as 256 terminals may be provided on the modified ATA bus 124 for interconnecting as many as 256 devices 128 to the modified ATA bus 124 and in turn to the controller 120. However, alterations to standard ATA hardware and signalling protocols would be required in order to operably interconnect such a large number of devices to a controller 120.~~

~~Briefly stated, the~~ devices **128** <u>each compare the selection identifier to</u> ~~are modified as compared to a conventional ATA type device in that they are each assigned a different identifier, and in that they are adapted to compare a identifier received as part of a selection command to~~ the assigned identifier. ~~In a typical implementation, these modifications from a typical ATA device may be accomplished by modifying the firmware of the device 128.~~ For example, the devices **128** ~~may~~ <u>include</u> ~~be provided with~~

a processor with ~~having~~ firmware that ~~running thereon that includes instructions for~~ comparesing the selection ~~received~~ identifier to the assigned identifier. If a device **128** is selected (the selection identifier matches the assigned identifier), then it sends a confirmation signal over the ATA bus **124** to the controller **120**. The remaining devices **128** are not selected (the selection identifier does not match the assigned identifier) and disconnect from the ATA bus **124**. The controller **120** then exchanges information (such as commands and data) over the ATA bus **124** with the selected device **128**. The controller **120** can subsequently de-select the selected device **128** and select another device **128** by issuing another selection command with a different selection identifier over the data lines.

In an embodiment, the controller **120** is a conventional ATA controller with modified firmware, the ATA bus **124** is a conventional ATA bus with eight edge connectors, and the devices **128** are conventional ATA devices with modified firmware. In another embodiment, the controller **120** is a conventional ATA controller with modified firmware and additional hardware (such as control registers and logic gates), the ATA bus **124** is a conventional ATA bus with eight edge connectors and additional hardware (such as separate DASP, PDIAG and INTRQ lines for each edge connector), and the devices **128** are conventional ATA devices with modified firmware. In yet another embodiment, the devices **128** determine whether the additional hardware is present and respond to the selection command based on the determination.

In an embodiment, the controller **120** selects the devices **128** by asserting a single selected data line, and the ATA bus **124** includes N data lines and N edge connectors. In this instance, the ATA bus **124** can support as many as N devices **128**. In another

embodiment, the controller **120** selects the devices **128** by sending a binary number across the data lines, and ATA bus **124** includes N data lines, N DASP lines, N PDIAG lines, N INTRQ lines, 2^N edge connectors and decoding logic that converts the DASP, PDIAG and INTRQ signals at the edge connectors into a binary number that is sent across the data lines to the controller **120**. In this instance, the ATA bus **124** can support as many as 2^N devices **128**.

~~Furthermore, the firmware may be configured such that a device **128** is disconnected from the modified ATA bus **124** if it is not selected. If a device **128** is selected, the firmware may cause a confirmation signal to be passed from that device to the controller **120** over the modified ATA bus **124**.~~

~~In the embodiment illustrated in **Fig. 1**, eight devices **128a-128h** are shown. Accordingly, the modified ATA bus system **104** illustrated in **Fig. 1** may be configured as a system **104** to which as many as eight devices **128** may be operatively interconnected to a single channel of the controller **120**. Alternatively, the embodiment illustrated in **Fig. 1** could be one in which as many as 256 devices **128** may be connected, but that has only eight devices **128** installed. As can be appreciated by one of skill in the art, by selectively asserting one bit of an eight bit selection command or word, a particular device **128** from a group of eight such devices **128** may be selected. Furthermore, it can be appreciated that one device **128** from among 256 devices **128** may be selected using a binary number defined by an eight bit identifier or selection command. Accordingly, using an 8 bit bus, a command sent over such a bus using an 8 bit identifier may select from among 256 devices **128**.~~

~~The devices **128** may include any device capable of communicating across an~~

~~ATA bus that has been modified as described herein **124**. In a typical implementation, the devices **128** include storage devices. For example, the devices **128** may include hard disk drives, floppy disk drives, optical drives and tape drives.~~

~~The devices **128** are each assigned a different identifier. The identifier may be assigned through hardware or software. For example, jumpers provided on an exterior of each device **128** may be used to assign an identifier to the devices **128**. Alternatively, an identifier may be assigned by setting software switches during initialization of the devices **128**.~~

~~With reference to~~ **Fig. 2**~~,~~ illustrates ~~steps taken to~~ power~~-~~up of the bus~~a modified~~ ~~ATA~~ system **10~~6~~4** ~~in accordance with an embodiment of the present invention are illustrated~~. Initially, ~~at step **200**,~~ the power is turned on (step **200**). ~~At step **204**,~~ The devices **128** that are not logical unit zero (~~*i.e.* that are~~ not designated as the~~a~~ master) tristate ~~configure their~~ data lines, ~~bus drivers and drivers for the~~ INTRQ and PDIAG ~~signal lines~~(step **204**). To tristate a signal line means that the device **128** sets its driver for that signal line ~~to~~ a high impedance condition, as is well-known under the ATA protocol. The device **128** ~~drive~~ that is ~~has been assigned~~ the logical unit zero then tristates ~~configures its~~ PDIAG ~~driver to a high impedance condition~~ (step **208**).

A ~~t step **212**, a~~ determination is made as to whether ~~the~~ PDIAG ~~signal line provided as part of the ATA bus **124**~~ has been negated (the devices **128** have all tristated PDIAG) (step **212**). If not~~it has not been negated~~, the bus system **106** waits ~~at step **212**~~. If so, ~~the PDIAG signal line has been negated, (i.e., all of the devices **128** attached to the bus **124** have configured their driver for the PDIAG signal line in a high impedance condition) the system proceeds to step **216**. At step **216**,~~ the device **128** that is logical

unit zero asserts ~~the~~ PDIAG~~-~~, clears its ~~signal on the bus **124**. The device that is logical unit zero also negates the~~ BSY (busy) bit in its status register~~,~~ and sets its ~~asserts~~ DRDY (device ready) bit in its~~the~~ status register (step **216**) ~~of the device 128~~. A~~t step **220**, a~~ determination is then made as to whether the BSY bit is clear~~negate~~d and the DRDY bit is set (step **220**)~~asserted~~. If not~~this condition is not met~~, the ~~modified ATA~~ bus system **1064** waits ~~until the condition is satisfied~~. If so~~Once the condition is satisfied~~, power-up of the ~~modified ATA~~ bus system **1064** is complete (step **224**).

~~With reference now to~~ **Fig. 3**~~,~~ is a flowchart illustrating the response of a device **128** to a selection command ~~in accordance with an embodiment of the present invention is illustrated~~. Initially, ~~at step **300**,~~ a ~~device~~ selection command that includes a selection identifier is sent ~~received~~ on ~~the~~ data lines~~bus~~ of the ~~modified~~ ATA bus **124** (step **300**). E~~At step **304**,~~ each device **128** determines whether the selection identifier matches its assigned identifier (step **304**) ~~matches the identifier transmitted as part of the drive selection command~~.

If a device **128** determines that the selection identifier matches its assigned identifier~~there is a match~~, the selected device **128** next determines whether the ~~modified ATA~~ bus system **1064** ~~is~~ includes additional ~~using~~ hardware ~~registers~~ (step **308**). In particular, ~~That is,~~ the selected device **128** determines whether ~~whether registers such as may be provided as part of~~ the controller **120** includes additional control registers~~are being utilized for conveying certain information regarding the modified ATA bus system **104**~~. ~~If so, the modified ATA bus system **104** is being used in connection with hardware registers,~~ the selected device **128** enables its data lines~~bus~~ drivers (step **312**) and asserts ~~the~~ DASP ~~signal~~ (step **316**).

If notthe modified ATA bus system 104 is not configured for use with hardware registers, the selected device **128** tristates configures its PDIAG signal line driver in a high impedance condition (step **320**). At step **324**, the selected device **128** determines whether the PDIAG isignal line has been negated and . The selected device **128** idles at step **324** until the PDIAG isignal line has been negated (step **324**).

Once the PDIAG isignal line has been negated, the selected device **128** asserts the PDIAG signal (step **328**). In addition, the selected device **128** enables its data linebus and INTRQ drivers (step **332**) and asserts the INTRQ signal (step **336**).

If a device **128** determines at step **304** that the selection identifier does not match its assigned identifier (step **304**)the identifier assigned to that device **128** does not match the identifier specified as part of the selection command, the device **128** proceeds to step **340**. In step **340**, the device **128** determines whether the modified ATA bus system **1064** includes additional hardware (step **340**) registers. If sothe modified ATA bus system **104** uses hardware registers, the device **128** tristatesconfigures its the data linesbus drivers such that they present a high impedance to the data bus (step **344**) and the device **128** negates the DASP signal line (step **348**). If the modified ATA bus system **104** is not configured for use with hardware registers, the device **128** tristates the configures its data linesbus drivers, its INTRQ and its PDIAG drivers such that they present a high impedance to the respective data or signal lines (step **352**).

With reference now to **Fig. 4**, is a flowchart illustrating the selection of a device **128** in the connection with a modified ATA bus system **1064** without the additional hardwarein accordance with the present invention that does not utilize hardware in addition to that normally supplied with a conventional ATA bus is illustrated. Initially, at

~~step 400,~~ the host computer ~~system~~ 10~~4~~6 issues a ~~device~~ selection command that includes a selection identifier through the controller **120** to select ~~a~~ one of the devices **128** (device n) (step **400**). ~~The device selection command is issued through the controller **120.**~~ The devices **128** ~~all~~ receive the selection command over the data lines~~bus~~ of the ATA bus ~~or~~ ~~channel **124** of the modified ATA system **104**~~ (step **404**). The devices **128** ~~that are not selected (i.e.,~~ whose assigned identifiers do not match the selection identifier are not selected and ~~transmitting as part of the selection command) configure~~ tristate ~~their~~ data lines ~~bus drivers~~ and INTRQ ~~drivers such that they present a high impedance to the modified ATA bus **124** (step **408**). In addition, the devices **128** that are not selected~~ and negate ~~the~~ PDIAG ~~signal line~~ (step **408**).

The selected device **128** whose assigned identifier matches the selection identifier tristates ~~presents a high impedance at that devices' interconnection to the~~ PDIAG ~~signal line~~ (step **412**). ~~As noted above, the selected device **128** is that device having an assigned identifier matching the identifier transmitted with the selection command. At step **416**, the selected device **128**~~ determines whether ~~the~~ PDIAG ~~signal line~~ is negated and idles until PDIAG is negated (~~(step **416**). If it is not, the selected device **128** idles at~~ step **416**). Once~~If the~~ PDIAG ~~signal line~~ is negated, the selected device **128** asserts ~~the~~ PDIAG ~~signal,~~ and enables its data line~~bus~~ and INTRQ drivers (step **420**) and ~~. The selected device also~~ asserts ~~the~~ INTRQ ~~signal~~ (step **424**).

~~At step **428**, t~~The controller **120** determines whether ~~the~~ INTRQ i~~signal has been~~ asserted (step **428**). If not, the controller **120** waits. If so~~yes, the system host **106**, through~~ the controller **120**, reads the status register in the selected device **128** to verify the successful selection of the selected device **128** (step **432**). The host computer ~~system~~

1046 ~~may~~ then issues an additional commands, such as ~~commands~~ to send or receive data, through the controller **120** to the selected device **128** ~~through the controller **120**~~ (step **436**). Following a read/write command to send or receive data, data may be transferred ~~passed~~ between the controller **120** and the selected device **128**.

~~With reference now to **Fig. 5**,~~ shows the additional hardware in the ~~that may be provided in connection with a modified ATA~~ bus system **1064** ~~in accordance with the present invention is illustrated in block diagram form~~.

~~–~~The controller **120** includes the ~~Shown in **Fig. 5** are the modified ATA bus **124** and various~~ control registers **500**, ~~. In addition, **Fig. 5** shows~~ an AND gate **504**, an OR gate **508**, ~~,and~~ an interrupt request signal line **512**, an interrupt mask register bus **544** and an interrupt logic bus **548**.

The control registers **500** ~~generally~~ include a selected status register **516**, a ready status register **520**, an interrupt pending register **524**, and an interrupt mask register **528**. T~~As will be appreciated by those of skill in the art,~~ the ~~various~~ control registers **500** may be accessed through the register access address (control block register 4) and the register access data (control block register 5) under the ATA protocol. The AND gate **504** is eight two-input AND gates, the OR gate **508** has eight inputs and a single output, the interrupt request signal line **512** is a single signal line and the interrupt mask register bus **544** and the interrupt logic bus **548** are eight-bit buses.~~available as part of a conventional ATA controller. Furthermore, it will be appreciated that the AND gate **504**, OR gate **508** and interrupt request signal line **512** represent hardware that is not found in connection with a conventional ATA system, and that is unique to the modified ATA bus system **104** of the present invention.~~

The ATA bus **124** includes the data bus **502** that includes the data lines, the DASP bus **532** that includes eight DASP lines (DASP 0-7), the PDIAG bus **536** that includes eight PDIAG lines (PDIAG 0-7) and the INTRQ bus **540** that includes eight INTRQ lines (INTRQ 0-7). Thus, the data bus **502**, the DASP bus **532**, the PDIAG bus **536** and the INTRQ bus **540** are eight-bit buses.

The DASP lines, the PDIAG lines and the INTRQ lines are dedicated to the individual devices **128**. For example, DASP line 0, PDIAG line 0 and INTRQ line 0 are connected to device **128-0** and disconnected from devices **128-1** to **128-7**, DASP line 1, PDIAG line 1 and INTRQ line 1 are connected to device **128-1** and disconnected from devices **128-0** and **128-2** to **128-7**, and so on. Thus, unlike a conventional ATA bus which includes single DASP, PDIAG and INTRQ lines that are shared by the devices, the ATA bus **124** includes multiple DASP, PDIAG and INTRQ lines that are not shared by the devices **128**. Instead, the devices **128** are each connected to a separate DASP, PDIAG and INTRQ line.

The DASP bus **532** ~~**Fig. 5 illustratesis as**~~ an ~~an~~ input to the selected status register **516** ~~**the DASP signal bus 532.**~~ Accordingly, ~~the DASP pin of~~ each device **128** ~~of the modified ATA system **104 may**~~ selectively drives a corresponding DASP ~~signal~~ line on the DASP ~~signal~~ bus **532** to set a corresponding bit in the selected status register **516**. For example, device **128-0** selectively drives DASP line 0 to set a corresponding bit in the selected status register **516**, device **128-1** selectively drives DASP line 1 to set a corresponding bit in the selected status register **516**, and so on.

The PDIAG bus **536** is an input to the ready status register **520** ~~is the PDIAG signal bus 536~~. Accordingly, e~~E~~ach device **128** ~~included in the modified ATA bus system~~

~~104 may~~ selectively drives ~~the~~ a corresponding ~~individual~~ PDIAG ~~signal~~ line on the PDIAG bus **536** to set a corresponding bit in the ready status register **520**~~associated with that device 128. Accordingly, each device 128 is individually interconnected to the ready status register 520 by a dedicated signal line on the PDIAG signal bus 536 such that each device may selectively set a bit in the ready status register 520~~. For example, device **128-0** selectively drives PDIAG line 0 to set a corresponding bit in the ready status register **520**, device **128-1** selectively drives PDIAG line 1 to set a corresponding bit in the ready status register **520**, and so on.

The INTRQ bus **540** is an input to the interrupt pending register **524** ~~is the IRQ signal bus 540~~. Accordingly, e~~E~~ach device **128** ~~may~~ selectively drives a corresponding ~~the individual~~ INTRQ ~~signal~~ line on the INTRQ bus **540** to set a corresponding bit in the interrupt pending register **524**~~associated with it. Accordingly, the IRQ signal bus 540 provides an individual IRQ signal line for each device 128 included in the modified ATA system 104. The IRQ signal bus 540 is also interconnected to the AND gate 504, as will be described in greater detail below. Therefore, each device 128 may selectively set a bit in the interrupt pending register 524~~. For example, device **128-0** selectively drives INTRQ line 0 to set a corresponding bit in the interrupt pending register **540**, device **128-1** selectively drives INTRQ line 1 to set a corresponding bit in the interrupt pending register **540**, and so on.

~~As can be appreciated by one of skill in the art, the DASP signal bus 532, the PDIAG signal bus 536, and the IRQ signal bus 540 shown in Fig. 5 are 8 bit busses provided as part of the modified ATA bus 124, as is the data bus 502. Decode logic to set~~

~~the appropriate bit or bits in the registers **500** may be included as part of the hardware used to implement the modified ATA bus **124** of such an embodiment of the present invention. The decode logic may be provided using one or more field programmable gate arrays. Furthermore, it can be appreciated that if more than eight devices are to be supported by the modified ATA system **104**, alterations to the way in which the devices **128** drive the lines of the signal buses **532, 536** and **540** must be made. For example, each device **128** may be provided with an eight bit driver for each of the DASP, PDIAG, and IRQ signals, and may be interconnected to each of the data lines in the DASP **532**, PDIAG **536**, and IRQ **540** buses. As many as 256 devices **128** could then be connected to the modified ATA bus system **104**, provided that enough terminals are also provided for interconnecting the devices **128** to the modified ATA bus **124**. Alternatively, an individual signal line for each of the provided devices **128** must be provided by each of the DASP **532**, PDIAG **536**, and IRQ **540** signal buses, and a corresponding bit provided in the registers **500**. As many devices as signal lines and register bits were provided could then be connected to the modified ATA system **104**, provided that a like number of terminals were provided by the modified ATA bus **124**, and provided that alterations were made to the hardware and/or signalling protocols to accommodate increased signal path lengths.~~

The interrupt mask register **528** is written by the controller **120**. T~~As can be appreciated, t~~ypically, only one bit of the interrupt mask register **528** is~~will be~~ set and the remaining bits of the interrupt mask register **528** are clear~~enabl~~ed. The set bit indicates which one of the devices **128** is the selected device **128**.

–The INTRQ bus **540** and the interrupt ~~A~~-mask register bus **544** are inputs to the

AND gate **504**. The INTRQ bus **540** provides interrupt requests from the devices **128** to the AND gate **504**, and the interrupt mask register **528** ~~provides a signal~~ indicate~~s~~ive the selected device **128** to the~~of the enabled bits in the interrupt mask register **528** to the AND gate **504**. The~~ AND gate **504** ~~is also provided with the signals from the IRQ signal bus 540. In a system **104** having as many as eight devices **128** interconnected thereto, both the IRQ signal bus **540** and the interrupt mask register bus **544** will be eight bits wide. Accordingly, the AND gate **504** will typically consist of eight two input AND gates.~~ The output of the AND gate **504** is sent across the interrupt logic bus **548** ~~provides the output from the AND gate **504**~~ to the input of the OR gate **508**, and the output of the OR gate **508** is sent across the interrupt request signal line **512** to the system bus **108** and in turn to the processor **112**. If a set ~~any one~~ bit of the interrupt mask register **528** matches an asserted signal ~~any one IRQ signal~~ on the INTRQ ~~signal~~ bus **540**~~,~~ then a signal line ~~at least one of the bits~~ on the interrupt logic bus **548** will be high, and therefore the output o~~from~~ the OR gate **508** will also be high and the interrupt request signal line **512** will pass the interrupt request to the processor **112**. Thus, a~~A~~ high signal from the OR gate **508** indicates that the~~at least one~~ selected device **128**, as confirmed by the selection stored in the interrupt mask register **528**, is generating an interrupt request. ~~Such request is provided to the host **106** over the interrupt signal line **512**.~~

In an alternative embodiment, the ATA bus **124** may include decode logic to set the appropriate bits in the control registers **500**, and each device **128** may be provided with a driver connected to each of the signal lines in the DASP bus **532**, the PDIAG bus **536** and the INTRQ bus **540**. That is, the DASP lines, the PDIAG lines and the INTRQ lines are shared by (rather than dedicated to) the individual devices **128**. For example,

DASP line 0, PDIAG line 0 and INTRQ line 0 are connected to devices **128-0** to **128-7**, DASP line 1, PDIAG line 1 and INTRQ line 1 are connected to devices **128-0** to **128-7**, and so on. Thus, unlike a conventional ATA bus which includes single DASP, PDIAG and INTRQ lines that are shared by the devices, the ATA bus **124** includes multiple DASP, PDIAG and INTRQ lines that are shared by the devices **128**. Furthermore, the selection command sent over the data bus **502** and the DASP, PDIAG and INTRQ signals sent over the DASP bus **532**, the PDIAG bus **536** and the INTRQ bus **540**, respectively, can be eight-bit binary words with 2^8 or 256 addresses. As a result, as many as 256 devices **128** can be connected to the ATA bus **124** provided the ATA bus **124** has 256 edge connectors and the hardware and/or signaling protocols are altered to accommodate increased signal path lengths.

The additional hardware also ~~In general, the use of additional hardware as illustrated in **Fig. 5** allows the modified ATA bus system **104** to manage interrupt requests from the devices **128**. In addition, the embodiment of the present invention illustrated in **Fig. 5**~~ provides the opportunity for ~~-~~overlapping commands across the devices **128**~~drives~~. The interrupt pending register **524** allows the processor **112** to identify each device **128** that has asserted INTRQ and therefore has a pending interrupt. For instance, if the device **128-0** asserts INTRQ line 0 and the device **128-1** asserts INTRQ line 1, thereby setting the corresponding two bits in the interrupt pending register **524**, the commands can be overlapped by issuing a first~~drive~~ command to the~~a~~ device **128-0**~~first drive~~ and before the first command~~ed~~ operation is completed issuing a second command to the device **128-1**~~a second drive~~.

~~In an embodiment in which additional hardware such as that illustrated in **Fig. 5** is~~

~~provided, the modified ATA bus 104 may operate according to a different protocol. With reference now to~~ **Fig. 6,** illustrates power-up of the bus system **106** with the additional hardware using an ~~the operation of an embodiment employing one such~~ alternative protocol ~~is illustrated in block diagram form~~. Initially, ~~at step 600,~~ the power ~~to the modified ATA bus system 104~~ is turned on (step **600**). Each device **128** asserts DASP w ~~W~~ithin a selected amount of time, for example from about 1-10 milliseconds~~, each device 128 interconnected to the modified ATA bus system 104 asserts its associated DASP signal line~~ (step **604**). ~~At step 608, e~~Each device **128** asserts ~~its~~ PDIAG ~~signal line,~~ and negates ~~its~~ DASP ~~signal line~~ when it ~~the device 128~~ is ready to receive a command (step **608**).

~~At step 612, t~~The controller **120** determines whether ~~all of~~ the devices **128** have negated ~~the~~ DASP (step **612**~~signal~~). If not, the controller **120** waits ~~until all devices 128 have negated their DASP signal line~~ (step **612**). If so, t~~T~~he controller **120** next determines whether ~~all of~~ the devices **128** have asserted PDIAG (step **616**). If ~~they have~~ not, the controller **120** may notify the processor **112**~~host system 106~~ of a problem or that fewer than the expected or possible number of devices **128** are connected, or wait until the devices **128** have ~~all~~ asserted PDIAG. After ~~all of~~ the devices **128** have asserted PDIAG, or after the controller **120** has been instructed or has decided to continue with less than all of the devices **128** asserting PDIAG, the host computer **10**~~4~~**6** may read or write to the ~~modified~~ ATA bus **12**~~0~~**4** through the controller **120** (step **620**).

~~With reference now to~~ **Fig. 7** is a flowchart illustrating~~,~~ the selection of a device **128** in the bus system **106** with the additional hardware using an alternative protocol~~accordance with an embodiment of the present invention utilizing the hardware~~

~~illustrated in Fig. 5 is shown~~. Initially, ~~at step 700,~~ the host computer~~system~~ **1046** issues a ~~first or device~~ selection command to select a device **128** (device n) (step **700**). The devices **128** receive the ~~device~~ selection command over the data lines of the data bus~~lines~~ **502** ~~of the modified ATA bus 124~~ (step **704**). The devices **128** that are not selected tristate the ~~configure their~~ data lines~~bus drivers to present a high impedance to the data bus 502,~~ and ~~configure their DASP driver so as to~~ negate ~~the~~ DASP ~~signal corresponding to that device 128~~ (step **708**). The

~~A~~ selected device **128** enables its data line~~bus~~ **502** drivers~~,~~ and asserts ~~its~~ DASP ~~signal~~ (step **712**). T~~At step 716, t~~he controller **120** determines whether only the intended device **128** is indicated as selected in the selected status register **516** (step **716**). If so~~Once the controller 120 has confirmed that only the selected device 128 is indicated as selected~~, the host computer~~system~~ **1046** may issue another~~second~~ command, for example a command to read or write data, to the selected device **128** through the controller **120** and over the ~~modified~~ ATA bus **124** (step **720**).

~~From the foregoing discussion, it can be appreciated that the cabling used to implement the modified ATA bus 124 of the present invention is similar to that of a conventional ATA buses cabling. Indeed, in an embodiment without the hardware illustrated in Fig. 5 that is in addition to that provided as part of a conventional ATA system, and to which no more than two devices 128 are to be attached, the cable implementing the modified ATA bus 124 may be identical to a conventional ATA bus cable. In order to connect additional drives to the modified ATA bus system 104, the cable of the modified ATA bus 124 need only be provided with additional terminals to allow the physical interconnection of such additional devices 128.~~

The ~~In accordance with one embodiment of the~~ present invention may include ~~; and in particular one that employs additional hardware such as is illustrated in Fig. 5,~~ a back plane for implementing the physical channel of the ~~modified~~ ATA bus **124**, particularly if the additional hardware is included ~~is provided~~. T~~In particular, t~~he back plane ~~is adapted to~~ minimizes the distance that signals must travel between the controller **120** and ~~any of~~ the ~~attached~~ devices **128**. T~~In accordance with one embodiment of the present invention, t~~he back plane also ~~is adapted to~~ minimizes the capacitance in the signal lines between the controller **120** and the ~~attached~~ devices **128**. The back plane may incorporate the DASP bus **532**, the PDIAG bus **536**, the INTRQ bus **540**, the decode logic associated with these buses, and the AND gate **504**, the OR gate **508**, the interrupt request signal line **512** and the interrupt logic bus **548** for interrupt management.

The present invention may also include a ~~A~~ frame~~work~~ for holding the ~~holding multiple~~ devices **128** in close proximity to one another ~~may therefore be beneficially provided in connection with an embodiment of the present invention~~. For example, a frame~~work~~ for holding eight hard disk drives (the devices ~~(i.e., eight devices 128)~~) having integrated connectors ~~to~~ allows each ~~of the~~ hard disk drives to be ~~inter~~connected to the ~~modified~~ ATA bus **124** in a modular fashion ~~may be provided~~. T~~In accordance with one embodiment of the present invention, t~~he frame~~work~~ is no taller than necessary in order to accommodate the eight hard disk drives. For example, the frame~~work~~ may result in a hard disk drive stack height of 8 ½ inches. ~~The back plane may also incorporate the DASP 532, PDIAG 536 and IRQ 540 signal busses, decode logic associated with those busses 532, 536 and 540, and components 504, 508, 512 and 548 for interrupt management that are in addition to or modified from components provided~~

~~as part of a conventional ATA bus~~

The foregoing discussion of the invention has been presented for purposes of illustration and description. Further, the description is not intended to limit the invention to the form disclosed herein. Consequently, variations and modifications commensurate with the above teachings, within the skill and knowledge of the relevant art, are within the scope of the present invention. The embodiments described herein are further intended to explain the best way presently known of practicing the invention and to enable others skilled in the art to utilize the invention in such or in other embodiments or with various modifications required by their particular application or use of the invention. It is intended that the appended claims be construed to include the alternative embodiments to the extent permitted by the prior art.

ABSTRACT

The present invention allows more than two devices to be connected to a single ATA bus. The devices are each assigned a unique identifier, and a controller selects a device by sending a selection command that includes a selection identifier across data lines of the ATA bus to the devices. The devices each receive the selection command and compare the selection identifier to the assigned identifier. The device which matches the selection identifier to its assigned identifier is selected, and the other devices are not selected.~~A method and apparatus for increasing the device count on an ATA bus are provided. The present invention provides a modified ATA bus, to which more than three devices may be interconnected. According to the present invention, a selection command is provided to devices interconnected to the bus over the bus data lines. The devices, upon receiving the selection command, compare an identifier included in or associated with the command to an assigned identifier. A device that is selected prepares to receive an additional command or data, while a device that is not selected disconnects itself from the databus. The present invention includes modifying an ATA controller to issue a drive selection command, and modifying an ATA device, such as a hard disk drive, to allow an identifier to be assigned to that device, and to respond appropriately to a selection command. The present invention further includes providing an interconnection, such as a cable, having terminals to allow more than two devices to be interconnected to a signal channel of a controller.~~